WHAT IS CLAIMED IS:

1. A semiconductor processing device formed on a semiconductor substrate comprising:

a central processing unit;

an SRAM-type field programmable gate array which establishes a logic circuit based on logic building data written thereto;

a nonvolatile memory which stores the logic building data establishing the logic circuit in the SRAM-type field programmable gate array; and

a configuration circuit which implements a configuration operation for said SRAM-type field programmable gate array by using the logic building data stored in said nonvolatile memory,

wherein said configuration circuit includes a function of transferring the logic building data in said nonvolatile memory to said SRAM-type field programmable gate array at the event of power-on reset.

2. A semiconductor processing device according to claim 1, wherein said configuration circuit includes a function of releasing the internal reset signal on completion of configuration operation.

3. A semiconductor processing device according to claim 2, wherein said nonvolatile memory includes an exclusive bus for transferring the logic building data to said configuration

circuit at the time of configuration operation.

4. A semiconductor processing device according to claim 1, further including:

a terminal which indicates the completion of the configuration operation by said configuration circuit; and

a function of initiating a peripheral semiconductor device through said terminal.

5. A semiconductor processing device according to claim 1, wherein said nonvolatile memory comprises a flash memory.

6. A semiconductor processing device formed on a semiconductor substrate comprising:

a central processing unit;

an SRAM-type field programmable gate array which establishes a logic circuit based on logic building data written thereto;

a nonvolatile memory which stores the logic building data establishing the logic circuit in the SRAM-type field programmable gate array; and

a configuration circuit which implements a configuration operation for said SRAM-type field programmable gate array by using the logic building data stored in said nonvolatile memory,

wherein said configuration circuit includes a function of reconstructing, during the operation of said central processing unit, part of the logic building data in said

SRAM-type field programmable gate array which has been transferred from said nonvolatile memory.

7. A semiconductor processing device according to claim 6, wherein said nonvolatile memory comprises a flash memory.

8. A semiconductor processing device formed on a semiconductor substrate comprising:

a central processing unit;

an SRAM-type field programmable gate array which establishes a logic circuit based on logic building data written thereto;

a nonvolatile memory which stores the logic building data establishing the logic circuit in the SRAM-type field programmable gate array;

a configuration circuit which implements a configuration operation for said SRAM-type field programmable gate array by using the logic building data stored in said nonvolatile memory; and

a plurality of terminals in correspondence to the logic building data of said SRAM-type field programmable gate array,

wherein said configuration circuit includes a function of selecting logic building data in said nonvolatile memory in correspondence to said terminals and transferring the selected data to said SRAM-type field programmable gate array.

9. A semiconductor processing device according to claim 8, wherein said nonvolatile memory comprises a flash memory.

10. A semiconductor processing device formed on a semiconductor substrate comprising:

a central processing unit;

an SRAM-type field programmable gate array which establishes a logic circuit based on logic building data written thereto;

a nonvolatile memory which stores the logic building data establishing the logic circuit in the SRAM-type field programmable gate array; and

a configuration circuit which implements a configuration operation for said SRAM-type field programmable gate array by using the logic building data stored in said nonvolatile memory,

wherein said configuration circuit includes a register which stores a plurality of data corresponding to the logic building data of said SRAM-type field programmable gate array, and

wherein said configuration circuit includes a function of selecting logic building data in said nonvolatile memory in correspondence to the data in said register and transferring the selected data to said SRAM-type field programmable gate array.

11. A semiconductor processing device according to claim 10, wherein said nonvolatile memory comprises a flash memory.